REMARKS/ARGUMENTS

Claims 1-30 and 66-104 are pending in the application, with claims 1, 66, and 96-99 being the independent claims. Claims 1, 66, and 96, 99 and 101-104 have been amended, while claims 92 and 94 have been cancelled. Applicant reserves the right to pursue these and other claims in this and other applications.

Claims 92 and 94 stand rejected under 37 C.F.R. 1.75(c) as being of improper dependent form. In response, claims 92 and 94 have been cancelled.

Claims 66-104 stand rejected under 35 U.S.C. 112(2) as being indefinite. In response, the claims have been amended and the following explanation is provided. The term "non-substrate area" (top of page 2) has been deleted. The term "layer" corresponds to the layer 60 of the first embodiment which is described on pages 7-10 of the specification. The term "film" corresponds to the film 60 of the third and fourth embodiments which are described on pages 13-15 of the specification. Finally, the term "conductive" has been amended to "electrically conductive".

Claim 96 stands rejected under 35 U.S.C. 102(b) as being anticipated by Osorio (USPN 5,317,107). This rejection is respectfully traversed. Amended claim 96 recites a semiconductor device comprising:

> a semiconductor substrate;
>
> at least one electrical element fabricated on said substrate; and
>
> an electrically conductive unbiased layer provided on a backside of said substrate, said conductive layer **forming an electrical path for removing unwanted voltages and electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate.** (Emphasis added.)

In the rejection of claim 96, the Office Action asserted that Osorio discloses a conductive layer (adhesive) 48 "forming an electrical path between said substrate die and at least one non-substrate area" (Office Action, page 5, first paragraph). However, Osorio does not describe adhesive 48 as electrically connecting the substrate (die 46) to anything. Additionally, Osorio explicitly discloses a wire bond 50 extending from a power supply terminal to electrically connect a the metal base 16 with the power supply terminal of the die 46 (page 4, lines). Consequently, Osorio contains no disclosure or suggestion that the purpose of the adhesive 48 is to form an electrical path, as claimed.

Furthermore, the Office Action alleges that Osorio's wire bond 50 corresponds to the claimed "at least one electrical element". This assertion is also respectfully traversed. The specification states that the present invention relates to **semiconductor** electrical elements in general, such as transistors, resistors, capacitors, electrodes, amplifiers, inverters, and gates (page 7, lines 5-7, emphasis added). Thus, a passive, non-semiconductor component such as Osorio's wire bond 50 cannot correspond to the claimed electrical element. This is also the subject matter of claims 2 and 67. For at least the above reasons, the rejection of claim 96 as well as all claims dependent therefrom should be withdrawn.

Claims 1-3, 5, 8, 22, 29-30 and 97 stand rejected under 35 U.S.C. 102(a) as being anticipated by Burr (USPN 6,048,746). This rejection is respectfully traversed. The amended claim 1 recites a semiconductor device comprising:

> a semiconductor substrate;
>
> at least one electrical element circuit fabricated on an upper side of said substrate;
>
> a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to said substrate; and
>
> an electrically conductive unbiased layer provided on a back side of said substrate **for removing unwanted voltages and electrical**

noise from said substrate to maintain a uniform bias voltage throughout the substrate. (Emphasis added.)

Burr does not disclose "an electrically conductive layer provided on a back side of said substrate for removing unwanted voltages and electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate" as highlighted above. This is a crucial feature of the present invention (see specification, page 6, line 14 through page 7, line 1). Indeed, Burr is entirely silent on the issue of unwanted voltages and electrical noise, or maintaining a uniform bias voltage throughout a substrate. Contrary to the present invention, Burr discloses back side biasing (col. 1, line 45) for tuning the threshold voltage of a device; i.e. the potential between a device's substrate and source. The conductive layer in the present invention is unbiased and is used for a wholly different purpose. None of the other references applied by the Examiner disclose or suggest the above-noted features of the present invention. Claims 66 and 96-104 have been amended to recite these same features. Accordingly, the rejection of claims 1, 66, 96-104 and all claims dependent therefrom should be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By _____

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Version With Markings to Show Changes Made

Please amend the claims as follows:

1. (Amended) A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element circuit fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to said substrate; and

[a conductive] an electrically conductive unbiased layer provided on a back side of said substrate for removing unwanted voltages and electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate.

66. (Amended) A processor system comprising:

a processor;

a memory device in electrical communication with said processor;

at least one of said memory device and said processor comprising:

a semiconductor substrate;

at least one electrical element fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to said substrate; and

[a conductive] an electrically conductive unbiased layer provided on a back side of said substrate for removing unwanted voltages and electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate.

92. (Cancel without disclaimer or prejudice)

94. (Cancel without disclaimer or prejudice)

96. (Amended) A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on said substrate; and

[a] an electrically conductive unbiased layer provided on a backside of said substrate, said conductive layer forming an electrical path [between said substrate and at least one non-substrate area of said device] for removing unwanted voltages and electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate.

97. (Amended) A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate; and

[a] an electrically conductive unbiased layer provided on a backside of said substrate, said conductive layer forming an electrical path between said substrate and said bias voltage source thereby removing unwanted voltages and electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate.

98. (Amended) A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate;

[a] an electrically conductive unbiased metallic layer provided on a backside of said substrate, said conductive metallic layer wire bonded to a bonding pad of said

semiconductor device for removing unwanted voltages and electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate; and

said bonding pad forming an electrical path between said conductive metallic layer and at least one other area of said device.

99. (Amended) A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate; and

[a] an electrically conductive unbiased layer provided on a backside of said substrate, said conductive layer in electrical communication with a bonding pad of said semiconductor device for removing unwanted voltages and electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate.

101. (Amended) A processor system comprising:

a processor;

a memory device in electrical communication with said processor;

at least one of said memory device and said processor comprising:

a semiconductor substrate;

at least one electrical element fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to said substrate, said bias voltage distribution regions including an electrically conductive plug and a metallization layer; and

[a] an electrically conductive unbiased layer provided on a back side of said substrate for removing unwanted voltages and electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate.

102. (Amended) A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate, said bias voltage distribution regions including an electrically conductive plug and a metallization layer; and

[a] an electrically conductive unbiased layer provided on a backside of said substrate, said conductive layer forming an electrical path between said substrate and said bias voltage source for removing unwanted voltages and electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate.

103. (Amended) A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate, said bias voltage distribution regions including an electrically conductive plug and a metallization layer;

[a] an electrically conductive unbiased metallic layer provided on a backside of said substrate, said conductive metallic layer wire bonded to a bonding pad of said semiconductor device; and

said bonding pad forming an electrical path between said conductive metallic layer and at least one other area of said device for removing unwanted voltages and electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate.

104. (Amended) A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate, said bias voltage distribution regions including an electrically conductive plug and a metallization layer; and

[a] an electrically conductive unbiased layer provided on a backside of said substrate, said conductive layer in electrical communication with a bonding pad of said semiconductor device for removing unwanted voltages and electrical noise from said substrate to maintain a uniform bias voltage throughout the substrate.